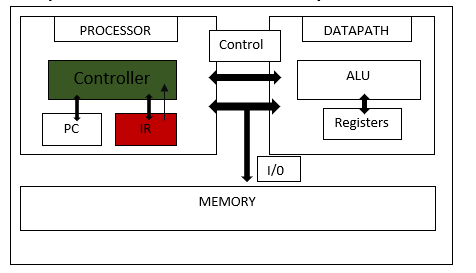
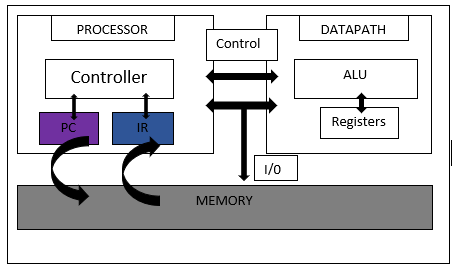
**VIRTUAL 8086 PROCESSOR**

|  |  |
| --- | --- |
| **Operations** | **Opcode** |
| **MOV** | 100010 |
| **ADD** | 000000 |
| **SUB** | 000101 |
| **DEC** | 111111 1 |
| **INC** | 111111 1 |
| **NOT** | 111101 1 |
| **AND** | 001000 |
| **OR** | 000010 |
| **CMP** | 001110 |
| **NEG** | 111101 1 |
| **XOR** | 000110 |
| **NOP** | 100100 00 |

|  |  |
| --- | --- |
| **Registers** | **Opcode** |
| **AX** | 000 |
| **AL** | 000 |
| **AH** | 000 |
| **BX** | 011 |
| **BL** | 011 |
| **BH** | 011 |
| **CX** | 001 |
| **CL** | 001 |
| **CH** | 001 |
| **DX** | 010 |
| **DL** | 010 |
| **SI** | 110 |
| **DI** | 111 |
| **BP** | 101 |
| **SP** | 100 |

**“MOV”**

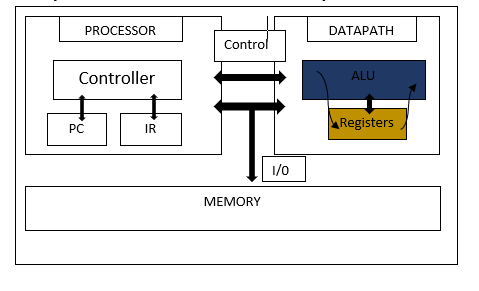
**(register to register) – 3 clock cycles**

****

DECODE

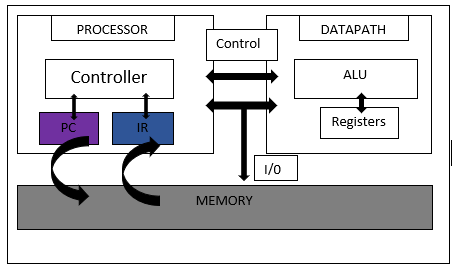
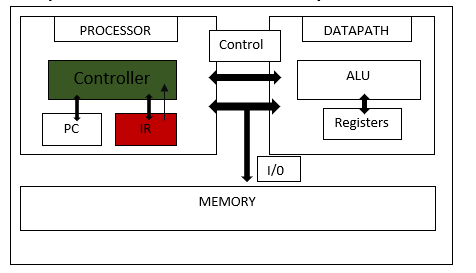
FETCH

EXECUTE

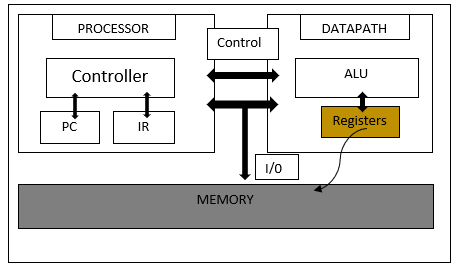
****

**“MOV”**

**(register to memory) – 3 clock cycles**

****

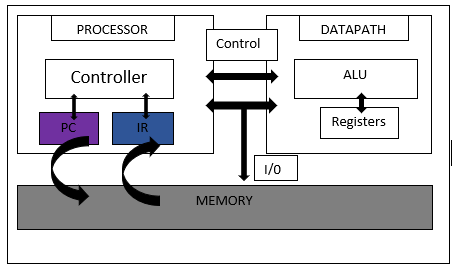
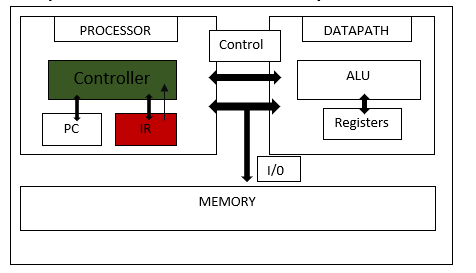
STORE

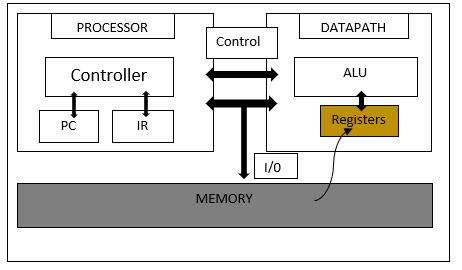
****

“MOV”

(memory to register) – 3 clock cycles

****

****

****

LOAD

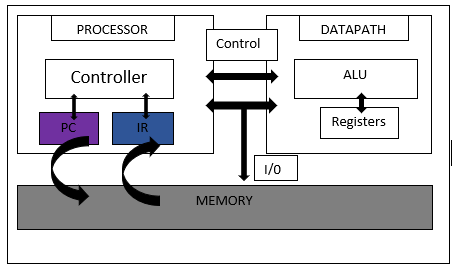
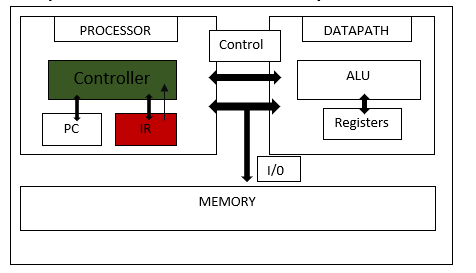
“ADD”

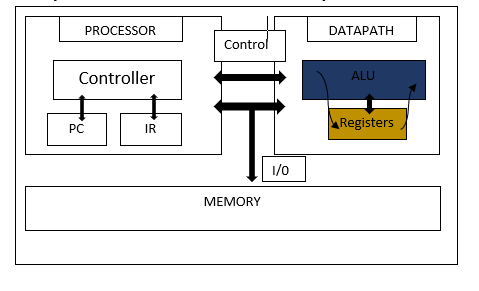
(register, register) – 3 clock cycles

“ADD”

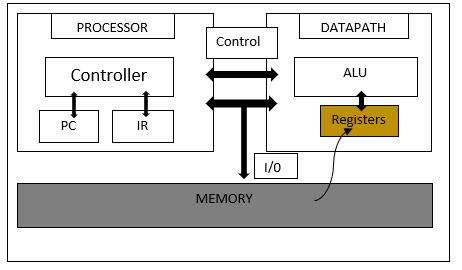
(register, memory) – 4 clock cycles

****

****

****

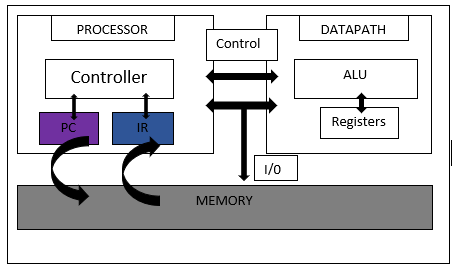
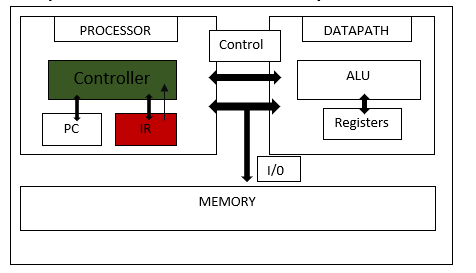
EXECUTE

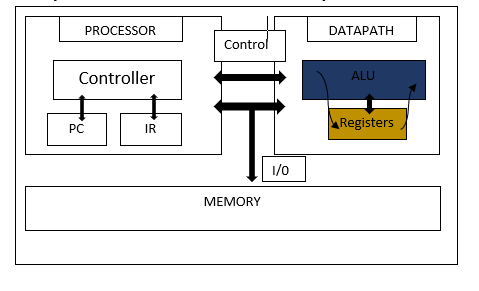
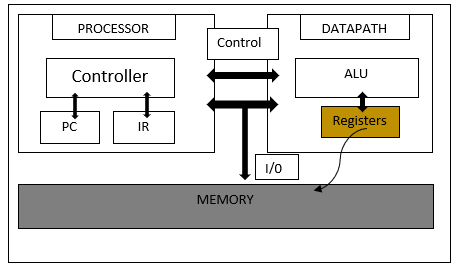
****

“ADD”

(memory, register) – 4 clock cycles

****

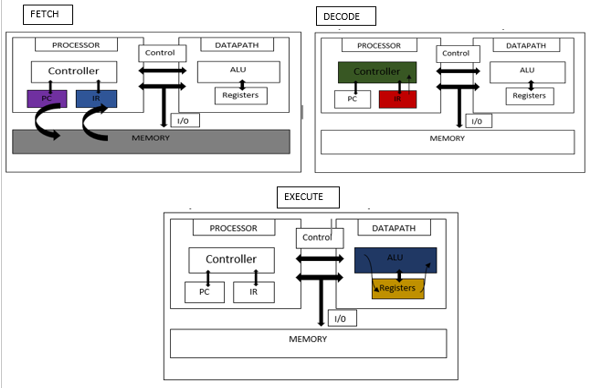
****

****

EXECUTE

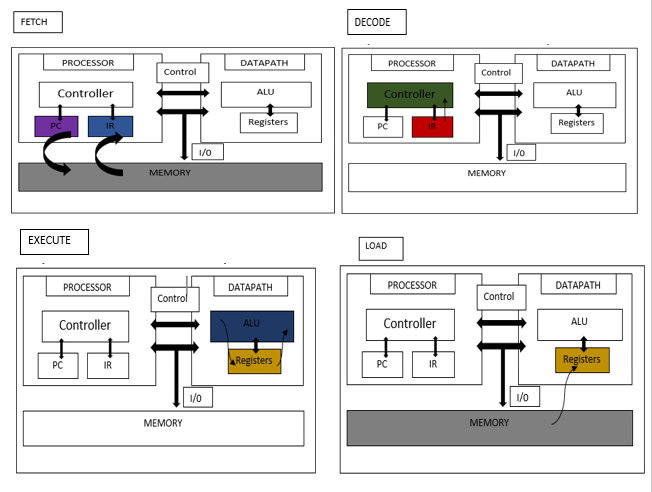
“SUB”

(register, register) – 3 clock cycles

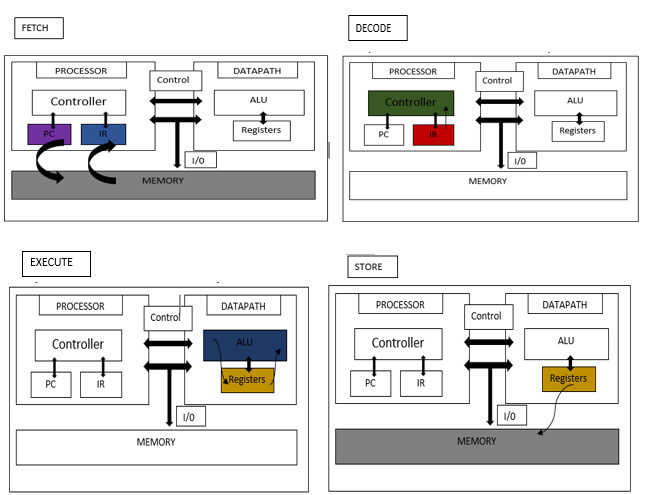


“SUB”

(register, memory) – 4 clock cycles



“SUB”

(memory, register) – 4 clock cycles

“INC”

(register) – 3 clock cycles

“INC”

(memory) – 3 clock cycles

“DEC”

(register) – 3 clock cycles

“DEC”  
(memory) – 3 clock cycles



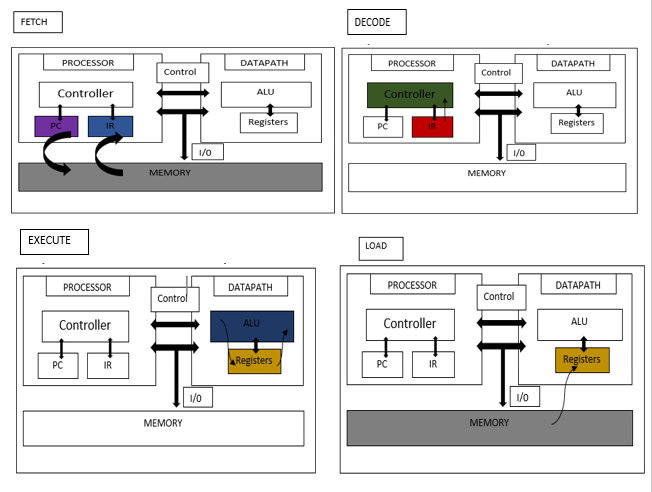
“AND”

(register, register) – 3 clock cycles

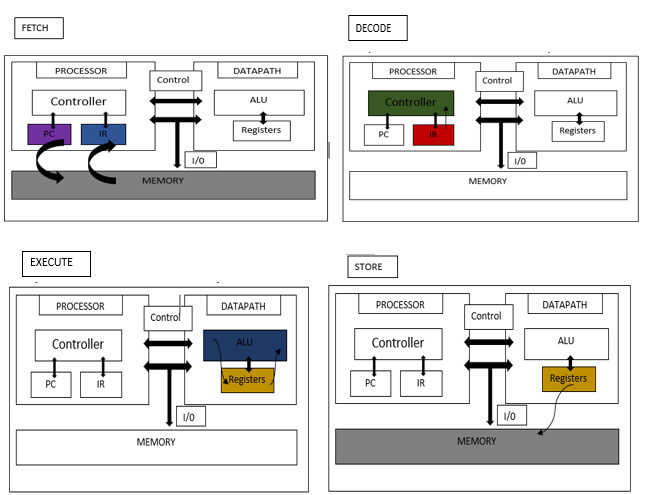


“AND”

(register, memory) – 4 clock cycles



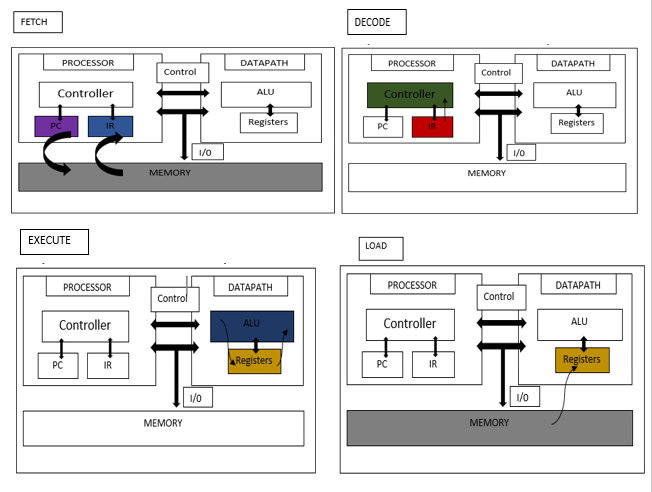
“AND”

(memory, register) – 4 clock cycles

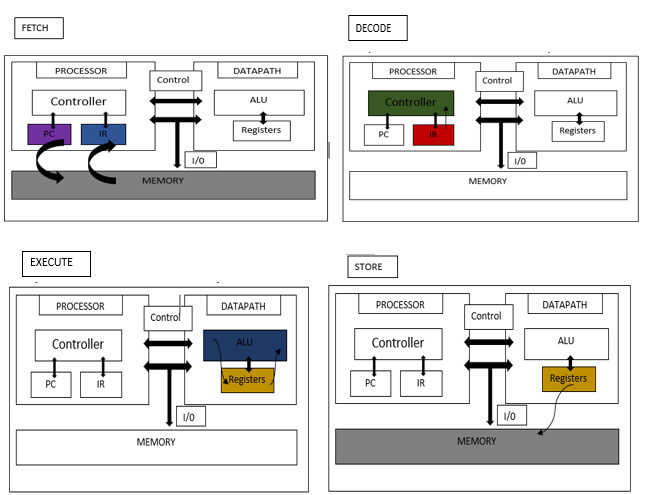
“OR”  
(register, register) – 3 clock cycles



“OR”  
(register, memory) – 4 clock cycles



“OR”

(memory, register) – 4 clock cycles

“NOT”  
(register) – 3 clock cycles



“NOT”  
(memory) – 3 clock cycles

“NEG”  
(register) – 3 clock cycles



“NEG”  
(memory) – 3 clock cycles

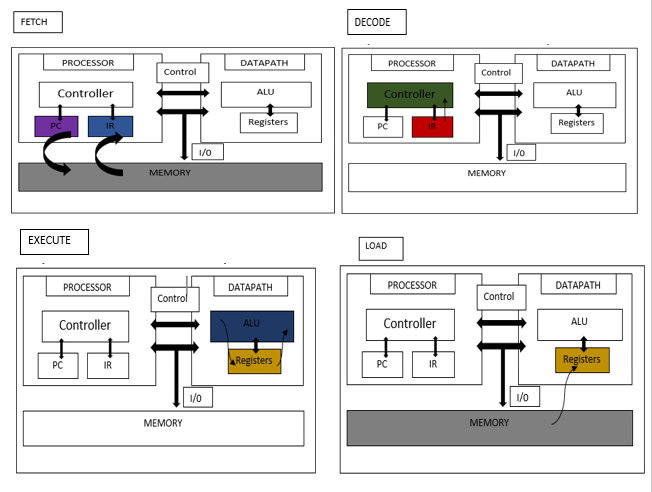


“XOR”

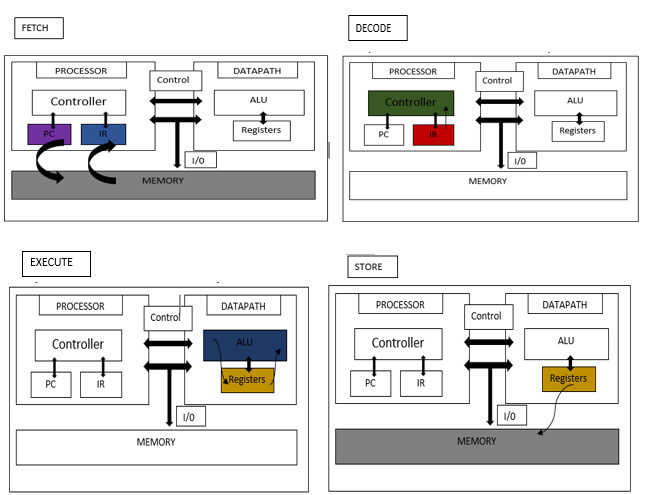
(register, register) – 3 clock cycles



“XOR”  
(register, memory) – 4 clock cycles



“XOR”  
(memory, register) – 4 clock cycles



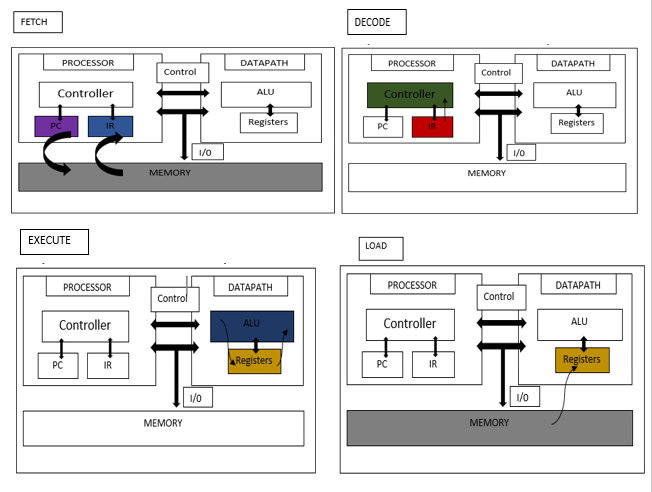
“CMP”

(register, register) – 3 clock cycles

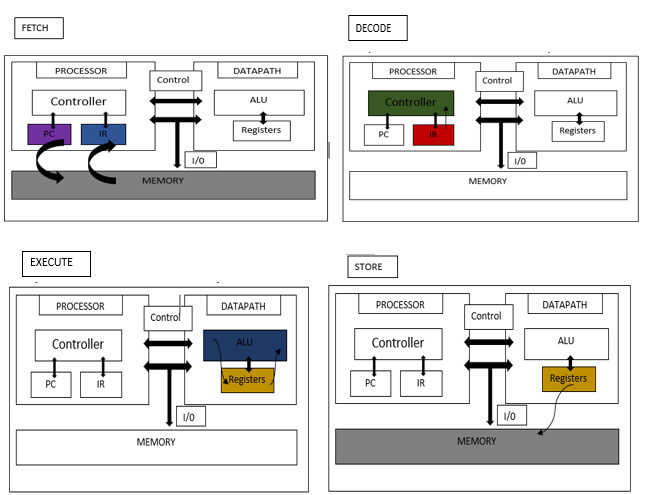


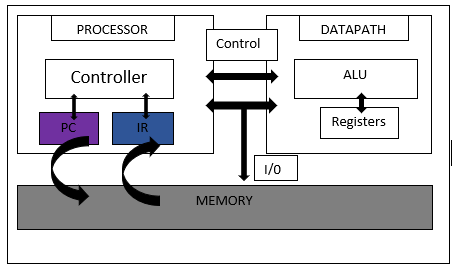
“CMP”

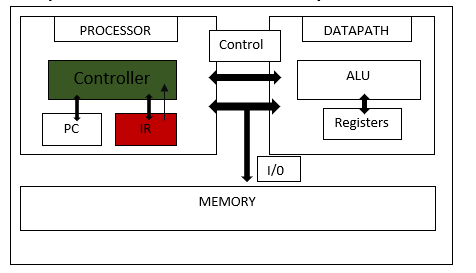
(register, memory) – 4 clock cycles



“CMP”

(memory, register) – 4 clock cycles

****“NOP”  
(register, register) – 2 clock cycles

****

“NOP”  
(memory, register) – 2 clock cycles

“NOP”  
(register, memory) – 2 clock cycles

